Terms used: **adc feedback filter**

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1 A methodology for efficient high-level dataflow simulation of mixed-s telecom transceivers

Gerd Vandersteen, Piet Wambacq, Yves Rolain, Petr Dobrovolný, Stéphane Bolsens

June 2000 **Proceedings of the 37th conference on Design automa**

Publisher: ACM Press

Full text available: pdf(241.33 KB) Additional Information: full citation, citings, inde

The explosion of the telecommunications market requires miniaturizatio realization of the front-ends of transceivers for digital telecommunicatio therefore be simulated at high level. Current methodologies and corresp common drawbacks, such as lower accuracy, slow simulation speed, etc been developped for the efficient simulation, at the architectural level, c of digital tel ...

2 Analogue and mixed-signal design and characterization: Experimen algorithm for high-speed filters

G. Matarrese, C. Marzocca, F. Corsi, S. D'Amico, A. Baschirotto

April 2007 **Proceedings of the conference on Design, automation a '07**

Publisher: ACM Press

Full text available: pdf(503.61 KB) Additional Information: full citation,

We report here the results of some laboratory experiments performed t of a technique for the self tuning of integrated continuous-time, high-sp tuning algorithm is based on the application of a pseudo-random input s pulses to the device to be tuned and on the evaluation of a few samples correlation function which constitute the filter signature.

The key advantages of this technique are th ...

3 A new algorithm for the design of stable higher order single loop sig converters

S. R. Kadivar, D. Schmitt-Landsiedel, H. Klar

December 1995 **Proceedings of the 1995 IEEE/ACM internationa Computer-aided design ICCAD '95**

Publisher: IEEE Computer Society

Full text available: pdf(341.91 KB) Publisher Site Additional Information: full citation, citings, inde

Abstract: This paper presents a new algorithm to attain optimized netw bit Sigma Delta Analog 1d Digital Converters (SD ADC) of order three o based on a novel mathematical description of stability and performance on the application of nonlinear interactive optimization techniques. The algorithm has been confirmed in practical implementations. The methoc correlation bet ...

Keywords: CAD, SD ADC, analogue-digital conversion, convertors, ele computing, higher order, network scaling, nonlinear interactive optimiz sigma delta analog-to-digital converters, single loop

4 Automotive: Low-g accelerometer fast prototyping for automotive ap

F. D'Ascoli, F. Iozzi, C. Marino, M. Melani, M. Tonarelli, L. Fanucci, A. Giam Marinis

April 2007 **Proceedings of the conference on Design, automation '07**

Publisher: ACM Press

Full text available: pdf(531.95 KB) Additional Information: full citation,

This paper presents an application of the ISIF chip (Intelligent Sensor I dual-axis low-g accelerometer in MEMS technology.

MEMS are nowadays the standard in automotive applications (and not o drastic reduction in cost, area and power, while they require a more cor with respect to traditional discrete devices. ISIF is a Platform On Chip ir fast prototype a wide range of automotive sensor ...

5 System architectures for computer music

John W. Gordon

June 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 2

Publisher: ACM Press

Full text available: pdf(4.61 MB) Additional Information: full citation, citings, inde

Computer music is a relatively new field. While a large proportion of the computer music in one form or another, there seems to be a need for a capabilities and limitations in terms of synthesis, performance, and recc addresses that need by surveying and discussing the architecture of exi systems. System requirements vary according to what the system will t for co ...

6 Energy efficient mobile computing: CMOS: a paradigm for low powe

Michiel Steyaert, Peter Vancorenland

June 2002 **Proceedings of the 39th conference on Design automa**

Publisher: ACM Press

Full text available: pdf(934.78 KB) Additional Information: full citation, index terms

An overview and comparison of different topologies for wireless architec the main focus lies on the power consumption and possibilities towards of external components. Architectures with reduced number of building external) are presented where the main benefits are the low costs, both as well as the power.

Keywords: CMOS, low-power, receivers, wireless

7 Future trends for wireless communication frontends in nanometer C

Georges G. E. Gielen

March 2007 **Proceedings of the 17th great lakes symposium on G on VLSI GLSVLSI '07**

Publisher: ACM Press

Full text available: pdf(450.37 KB) Additional Information: full citation, index terms

CMOS technology is evolving deeper and deeper into the nanometer era done in 90nm and even 65nm. This makes the integration of entire syst which are mixed-signal in nature, including analog and/or RF parts. The technology offers many opportunities for new telecom applications, such radios and wireless sensor networks. This invited paper first describes b for 4G radio frontends. This ...

Keywords: RF frontends, integrated circuits, reconfigurable hardware, wireless sensor networks

8 RF circuit design and design methodology: A 1GHz CMOS fourth-or bandpass sigma delta modulator for RF receiver front end A/D conv

K. Praveen Jayakar Thomas, Ram Singh Rana, Yong Lian

January 2005 **Proceedings of the 2005 conference on Asia South automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(661.92 KB) Additional Information: full citation,

A design and circuit implementation of a CMOS fourth-order continuous delta modulator is presented. The fully differential architecture of the m integrated LC resonators with active Q enhancement and return to zero to drive the feedback switched current source DACs. The modulator, de 1P6M CMOS process occupies a total area of 1.8mm^2 dissipating 290mV supp ...

9 Low power design and technology: A power optimized design metho sigma-delta-pipeline ADCs

Vahid Majidzadeh, Omid Shoaei

April 2006 **Proceedings of the 16th ACM Great Lakes symposium c**

Publisher: ACM Press

Full text available: pdf(2.04 MB) Additional Information: full citation, index terms

A power optimized design methodology for low-distortion sigma-delta-p The minimum power consumption of these converters for a given specif dynamically exploiting the slewing and partially settling regimes of the i dynamic expression for maximum possible output swing of the OTAs, w

factors. The proposed, precise, and yet simple approach gives in rapid a ADCs. In order to ve ...

Keywords: power optimization, reduced-sample-rate architectures, sig

10 Mixed-signal design and simulation: A 16-bit mixed-signal microsyst CMOS-MEMS clock reference

Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale, Fadi H. Get Matthew R. Guthaus, Richard B. Brown

June 2003 **Proceedings of the 40th conference on Design automa**

Publisher: ACM Press

Full text available: pdf(793.60 KB) Additional Information: full citation, citings, inde

In this work, we report on an unprecedented design where digital, analc are combined to realize a general-purpose single-chip CMOS microsyste these technologies has enabled the development of a low power, portat suited for controlling environmental and bio-implantable sensors.

Keywords: ADC, MEMS, PGA, SD, SoC, clock generation, design methc power, low voltage analog, microcontroller, microsystem, mixed-signal,

11 Automotive: Mixed-signal design of a digital input power amplifier fo applications

Sergio Saponara, Pierangelo Terreni

March 2006 **Proceedings of the conference on Design, automatio Designers' forum DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(355.73 KB) Additional Information: full citation,

With reference to digital input power amplifier for automotive audio app presents an exhaustive exploration of the huge mixed-signal space to fi among different cost-functions: distortion, efficiency, circuit complexity architectural solutions are modelled and compared in a Simulink/Spice f blocks (i.e. oversampling filter, noise shaping, type of PWM modulation, stage, LC filter) are ...

12 Methods and tools for systematic analogue design: Arbitrary design

transfer function for a novel class of reduced-sample-rate sigma-del
V. Majidzadeh, O. Shoaei
March 2006 **Proceedings of the conference on Design, automatio Proceedings DATE '06**
Publisher: European Design and Automation Association
Full text available: pdf(441.91 KB) Additional Information: full citation,

A novel noise transfer function (NTF) for high order reduced-sample-rat (SDP) ADCs is presented. The proposed NTF determines the location of improving the stabilization of the loop and implementing the reduced-sa concurrently. A design methodology based on simulated-annealing-algo design the optimum NTF. To verify the usefulness of the proposed NTF a different modulators are presented. Simul ...

13 Detection of defective sensor elements using ΣΔ -modulation and a
D. Weiler, O. Machul, D. Hammerschmidt, B. J. Hosticka
January 2000 **Proceedings of the conference on Design, automati DATE '00**
Publisher: ACM Press
Full text available: pdf(88.57 KB) Publisher Site Additional Information: full citation,

14 Poster session IV: A high performance QAM receiver for digital cabl and FEC decoder
Bo Shen, Junhua Tian, Zheng Li, Jianing Su, Qianling Zhang
January 2005 **Proceedings of the 2005 conference on Asia South automation ASP-DAC '05**
Publisher: ACM Press
Full text available: pdf(391.37 KB) Additional Information: full citation,

A DVB-C/ITU J.83-A compliant QAM (Quadrature Amplitude Modulation) digital cable TV is proposed, which can support 4~256QAM with variable integrates a 10-bit 40MSPS ADC, (204,188) Reed-Solomon decoder as v interleaver. The chip is implemented in SMIC 0.25um CMOS technology mm^2. It features wide carrier offset acquisition range, robust demodulat

circuit area.

15 Analog and mixed signal design: 4GHz continuous-time bandpass d directly high IF A/D conversion

A. A. Mariano, D. Dallet, Y. Deval, J-B. Begueret

August 2006 **Proceedings of the 19th annual symposium on Integ systems design SBCCI '06**

Publisher: ACM Press

Full text available: pdf(1.13 MB) Additional Information: full citation, index terms

We present in this article a fourth-order integrated LC bandpass Delta-S conversion of high intermediate frequencies. It is designed in a 0.25 µm from STMicroelectronics. The modulator is able to direct digitize a 1GHz bandwidth. The continuous-time loop filter employs two integrated LC r enhancement circuits. A multi-feedback architecture is used to achieve while maintaini ...

Keywords: A/D conversion, bandpass delta-sigma modulator, continuo modulator, high order noise-shaping, high-IF sampling, multi-feedback

16 A two-layer library-based approach to synthesis of analog systems f specifications

Alex Doboli, Nagu Dhanwada, Adrian Nunez-Aldana, Ranga Vemuri

April 2004 **ACM Transactions on Design Automation of Electronic S** Volume 9 Issue 2

Publisher: ACM Press

Full text available: pdf(658.00 KB) Additional Information: full citation, citings, inde

This paper presents a synthesis methodology for analog systems descril language. Synthesis produces net-lists of analog components that are s sized so that specified objectives (like AC response, signal to noise ratic optimized. The gap between abstract specifications and implementation layered methodology. The first layer is architecture generation. The sec synthesis and constrain ...

Keywords: Analog synthesis, VHDL-AMS, branch-and-bound, genetic a estimation

17 Combining software synthesis and hardware/software interface gen
time constraints
Steven Vercauteren, Jan Van Der Steen, Diederik Berkest
January 1999 **Proceedings of the conference on Design, automati DATE '99**
Publisher: ACM Press
Full text available: pdf(127.72 KB) Additional Information: full citation,

18 Pseudo-Random Sequence Based Tuning System for Continuous-T
F. Corsi, C. Marzocca, G. Matarrese, A. Baschirotto, S. D'Amico
February 2004 **Proceedings of the conference on Design, automa Volume 1 DATE '04**
Publisher: IEEE Computer Society
Full text available: pdf(173.78 KB) Additional Information: full citation,

Continuos-Time filters are widely used in signal processing but require a their frequency response. Several tuning techniques have been propose can be grouped in two basic schemes: master-slave and self-calibration propose a novel tuning approach which can be applied to both tuning sc algorithm is based on the application of a pseudo-random input Test Pa evaluation of a few samples of th ...

19 Area-efficient and reusable VLSI architecture of decision feedback e
modern
Hyeongseok Yu, Byung Wook Kim, Yeon Gon Cho, Jun-Dong Cho, Jea Woc Won Lee
January 2001 **Proceedings of the 2001 conference on Asia South automation ASP-DAC '01**
Publisher: ACM Press
Full text available: pdf(176.90 KB) Additional Information: full citation, index terms

In this paper, an area efficient VLSI architecture of decision feedback ec accommodating 64/256 QAM modulators. This architecture is implemen VLSI structure using EDA tool due to its regular structure. The main ide multiplexed design scheme grouping the adjacent filter taps with correl with data transfer having same processing sequence between blocks. W design scheme using SYN ...

20 Analogue and mixed-signal design: Double-sampling single-loop sig topologies for broadband applications

Mohammad Yavari, Omid Shoaei, Angel Rodriguez-Vazquez

March 2006 **Proceedings of the conference on Design, automatio Proceedings DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(250.76 KB) Additional Information: full citation,

This paper presents novel double sampling high order single-loop sigma for wideband applications. To alleviate the quantization noise folding int region, two previously reported techniques are used. The DAC sampling with the single capacitor approach and an additional zero is placed at th frequency of the modulator's noise transfer function (NTF). The detrime zero on both th ...

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	(A ADJ1 D or adc or analog ADJ1 digital) (pulse ADJ1 width ADJ1 modulated or pwm) time ADJ1 domain	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 10:39
L2	2	(A ADJ1 D or adc or analog ADJ1 digital) (pulse ADJ1 width ADJ1 modulated or pwm) time ADJ1 domain and aqm	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 09:48
L3	10	(A ADJ1 D or adc or analog ADJ1 digital) (pulse ADJ1 width ADJ1 modulated or pwm) flip ADJ1 flop	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 10:12
L4	259	(341/166).CCLS.	USPAT	OR	OFF	2007/06/27 09:53

EAST Search History

L5	61	l4 and flip ADJ1 flop	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 09:53
L6	2	(A ADJ1 D or adc or analog ADJ1 digital) oscillat$5 flip ADJ1 flop (feedback or back)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 10:15
L7	91	(A ADJ1 D or adc or analog ADJ1 digital) flip ADJ1 flop (feedback or back)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 10:21
L8	41617	"341".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:19

EAST Search History

L9	0	"341".ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:18
L10	0	"341".clas. and l9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:19
L11	41617	"341".clas. and l8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:19
L12	0	"341".ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:20

EAST Search History

L13	41617	"341".clas.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:20
L14	996	"341".clas. and delta.ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:20
L15	2000	(341/155).CCLS.	USPAT	OR	OFF	2007/06/27 10:21
L16	6	(A ADJ1 D or adc or analog ADJ1 digital) flip ADJ1 flop (feedback or back) and l15	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 10:22
L17	2	(A ADJ1 D or adc or analog ADJ1 digital) (pulse ADJ1 width ADJ1 modulated or pwm) time ADJ1 domain and cf	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 10:38

EAST Search History

L18	0	(A ADJ1 D or adc or analog ADJ1 digital) (pulse ADJ1 width ADJ1 modulated or pwm) time ADJ1 domain and flip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 10:39
L19	2	"20070085717"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 11:40
L20	2	"6232902".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:40
L21	1	"6232902".pn. and "d"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:41

EAST Search History

L22	2	"6232902".pn. and flip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:42
L23	0	"6232902".pn. ocillat$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:43
L24	1	"6232902".pn. sampl$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 11:11
L25	1	"6232902".pn. down	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:48

EAST Search History

L26	1	"6232902".pn. width	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:49
L27	1	"6232902".pn. filter	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:53
L28	2	"6232902".pn. "11"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:50
L29	1	"6232902".pn. filter$6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 10:53

EAST Search History

L30	1	"6232902".pn. and high sampl$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 11:15
L31	1	"6232902".pn. and bit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 11:19
L32	1	"6232902".pn. and latch$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 11:20
L33	1	"6232902".pn. and differential	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 11:25

EAST Search History

L34	1	"6232902".pn. and single	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 11:28
L35	0	"6232902".pn. and band	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 11:28
L36	1	"6232902".pn. and pass	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 11:29
L37	1	"6232902".pn. and limit$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 11:30

EAST Search History

L38	1	"6232902".pn. and transfer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 11:39
L39	0	"6232902".pn. and difference	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 11:39
L40	1	"20070085717" differential	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2007/06/27 11:41
L41	1	"20070085717" and single ended	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/27 11:47
L42	4813	(341/143,155,110,144, 166).CCLS.	USPAT	OR	OFF	2007/06/27 11:48

EAST Search History

L43	3289	(341/143,155).CCLS.	USPAT	OR	OFF	2007/06/27 11:48